CLAIMS

Having thus described our invention in detail, what we claim as new and desire to secure by the Letters Patent is:

1. A method of fabricating a SiGe-on-insulator substrate material comprising:

providing a structure comprising a Si-containing substrate having a hole-rich region formed therein and a Ge-containing layer atop the Si-containing substrate;

converting the one hole-rich region into a porous region; and

annealing the structure including the porous region to provide a substantially relaxed SiGe-on-insulator material.

2. The method of Claim 1 wherein the providing step comprises growing a p-rich epitaxial layer on an initial Si-containing substrate, forming a single crystal Si-containing layer atop the p-rich epitaxial layer, and forming the Ge-containing layer on the single crystal Si-containing layer.

3. The method of Claim 1 wherein the providing step comprises ion implanting a p-type dopant into an initial single crystal Si-containing substrate and then forming the Ge-containing layer on the substrate.

4. The method of Claim 3 wherein the p-type dopant is Ga, Al, B or BF_2.

5. The method of Claim 3 wherein the p-type dopant is B, said B is implanted at an energy of from about 100 keV to about 500 keV and a dose of about 5E15 atoms/cm^2 to about 5E16 atom/cm^2.

6. The method of Claim 3 wherein the p-type dopant is BF_2, said BF_2 is implanted at an energy of from about 500 keV to about 2500 keV and a dose of about 5E15 atoms/cm^2 to about 5E16 atom/cm^2.

7. The method of Claim 1 wherein the providing step comprises forming the Ge-containing layer on an initial single crystal Si-containing substrate and then implanting p-type dopant into the substrate to form said hole-rich region.

8. The method of Claim 1 wherein said hole-rich region has a p-type dopant concentration of about 1E19 atoms/cm^3 or greater.

9. The method of Claim 8 wherein said hole-rich region has a p-type dopant concentration of from about 1E20 atoms/cm^3 to about 5E20 atoms/cm^3.

10. The method of Claim 3 further comprising an annealing step.

11. The method of Claim 10 wherein the annealing step is selected from the group consisting of a furnace anneal, a rapid thermal anneal, and a spike anneal.

12. The method of Claim 11 wherein the annealing step is a furnace anneal step, said furnace anneal step is carried out at a temperature of about 600°C or greater for a time period of about 15 minutes or greater in the presence of an inert gas atmosphere, an oxidizing ambient or a mixture thereof.

13. The method of Claim 11 wherein the annealing step is a rapid thermal anneal (RTA) step, said RTA step is carried out at a temperature of about 800°C or greater for a time period of about 5 minutes or less in the presence of an inert gas atmosphere, an oxidizing ambient or a mixture thereof.

14. The method of Claim 11 wherein the annealing step is a spike annealing step, said spike annealing step is performed at a temperature of about 900°C or greater for a time period of about 1 second or less in the presence of an inert gas atmosphere, an oxidizing ambient or a mixture thereof.

15. The method of Claim 7 further comprising an annealing step.

16. The method of Claim 15 wherein the annealing step is selected from the group consisting of a furnace anneal, a rapid thermal anneal, and a spike anneal.

17. The method of Claim 16 wherein the annealing step is a furnace anneal step, said furnace anneal step is carried out at a temperature of about 600°C or greater for a time period of about 15 minutes or greater in the presence of an inert gas atmosphere, an oxidizing ambient or a mixture thereof.

18. The method of Claim 16 wherein the annealing step is a rapid thermal anneal (RTA) step, said RTA step is carried out at a temperature of about 800°C or greater for a time period of about 5 minutes or less in the presence of an inert gas atmosphere, an oxidizing ambient or a mixture thereof.

19. The method of Claim 16 wherein the annealing step is a spike annealing step, said spike annealing step is performed at a temperature of about 900°C or greater for a time period of about 1 second or less in the presence of an inert gas atmosphere, an oxidizing ambient or a mixture thereof.

20. The method of Claim 1 wherein the converting step comprising an electrolytic anodization process.

21. The method of Claim 20 wherein the anodization process is performed in the presence of a HF-containing solution.

22. The method of Claim 20 wherein the anodization process is performed using a constant current source operating at a current density of from about 0.05 to about 50 milliAmps/cm^2.

23. The method of Claim 1 wherein the porous region has a porosity of about 1% or greater.

24. The method of Claim 1 further comprising forming a cap layer atop the Ge-containing layer after said converting step, but prior to said annealing step.

25. The method of Claim 24 wherein the cap layer comprises a Si material.

26. The method of Claim 1 wherein the annealing step is performed in an oxygen-containing ambient.

27. The method of Claim 26 wherein the oxygen-containing ambient further comprises an inert gas.

28. The method of Claim 27 wherein the oxygen-containing ambient is selected from the group consisting of O_2, NO, N_2O, ozone, and air.

29. The method of Claim 1 wherein the annealing step is performed at a temperature of from about 650°C to about 1350°C.

30. The method of Claim 1 wherein the annealing step forms a surface oxide atop the substantially relaxed SiGe-on-insulator material.

31. The method of Claim 1 wherein the insulator of said SiGe-on-insulator material is a thermal oxide.

32. The method of Claim 1 further comprising forming a Si layer atop the substantially relaxed SiGe-on-insulator material.

33. The method of Claim 1 wherein the hole-rich regions are continuous.

34. The method of Claim 1 wherein the hole-rich region comprises discrete islands and said insulator of said substantially relaxed SiGe-on-insulator material comprises discrete islands of thermal oxide.

35. The method of Claim 1 further comprising repeating the providing, converting and annealing steps any number of times to provide a multi-layered SiGe-on-insulator material.

36. A method of fabricating a SiGe-on-insulator substrate material comprising:

providing a structure comprising a Si-containing substrate having a region of a high concentration of p-type dopant formed therein and a Ge-containing layer atop the Si-containing substrate;

converting the region of p-type dopant into a porous region using an anodization process, wherein an HF-containing solution is employed; and

oxidizing the structure including the porous region to provide a substantially relaxed SiGe-on-insulator material.